REMARKS

The Office Action dated December 29, 2006 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1-3, 5-7, and 11-13 have been amended to more particularly point out and distinctly claim the subject matter of the invention. New claim 15 has been added. No new matter has been added. Claims 8-10 and 14 have been withdrawn pursuant to an election of species requirement. Therefore, claims 1-7, 11-13 and 15 are respectfully submitted for consideration.

The Office Action rejected claims 1-7 and 11-13 under 35 U.S.C. §102(e) as being anticipated by Paul (U.S. Patent No. 6,704,863). The rejection is respectfully traversed for the following reasons.

Claim 1, upon which claims 2-7 are dependent, recites a method which includes performing a data transfer between a memory of a processor device and a circuitry connected to the processor device. The performing includes setting up at the circuitry a direct memory access for transferring data, triggering at the circuitry a direct memory access transfer of the data to the processor device, adding in the circuitry the direct memory access transfer to a transaction log, providing the transaction log from the circuitry to the processor device when the transaction log has reached a predetermined limit, and informing the processor device of the availability of the transaction log.

Claim 11, upon which claims 12 and 13 are dependent, recites an integrated circuit including functionality configured to provide access to a processor device. The integrated circuit is configured to set up a direct memory access for transferring data via the access means, to trigger a direct memory access transfer of the data, to add the direct memory access transfer to the transaction log, to provide the transaction log to the processor device when the transaction log has reached a predetermined limit, and to issue an information indicating the availability of the transaction log.

Therefore, according to embodiments of the invention, a pre-programmed direct memory access (DMA) located on interfaces hosted by the external circuitry is provided to transfer data between the memory and the external circuitry, wherein processor control requirements can be reduced by using the transaction log. Thus, a plurality of data transfers can be bundled with a single DMA operation, since the processor device may validate or qualify the transferred data based on the available transaction log, when the availability, e.g. transfer or interrogation, of the transaction log has been informed to the processor device. Since the processor device is only involved in the signaling of the information regarding the provision, e.g. transfer or interrogation, of the transaction log, interrupt overheads and associated core load can be significantly reduced. Furthermore, the need for manual data movement is prevented, and a data rate matching can be provided between the shared memory and the on-chip bus system of the external circuitry to thereby reduced stalling of the system (Specification, page 3, lines 22-34).

As will be discussed below, the cited prior art fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the advantages/features discussed above.

Paul discloses a method for servicing an interrupt in a pipelined processor, including generating one or more interrupt-related instructions within the processor in response to the interrupt and inserting the interrupt-related instructions into the pipeline of the processor for execution. These interrupt-related instructions generated within the processor may constitute the entire interrupt service routine, or alternatively, a portion of the interrupt service routine. Main program instructions which may be present in the instruction pipeline of the processor prior to receiving the interrupt are retained when the interrupt-related instructions are inserted. Normal operation of the pipeline may be resumed subsequent to execution of the interrupt-related instructions, beginning with execution of any main program instructions retained in the pipeline at the time of the interrupt.

Applicants respectfully submit that Paul fails to disclose or suggest all of the elements of the presently pending claims. For example, Paul does not disclose or suggest "setting up at said circuitry a direct memory access for transferring data; triggering at said circuitry a direct memory access transfer of said data to said processor device," as recited in claim 1. Similarly, Paul fails to disclose or suggest "functionality configured to provide access to a processor device, wherein said integrated circuit is configured to set up a direct memory access for transferring data via said access means, to trigger a direct

memory access transfer of said data, to add said direct memory access transfer to said transaction log," as recited in claim 11.

Paul, as discussed above, discloses low-latency DMA handling in pipelined processors. The processor includes interrupt handling circuitry adapted to generate one or more interrupt-related instructions in response to an interrupt signal, and insert the interrupt-related instructions into a pipeline of the processor for execution (Paul, Column 8, lines 26-45 and Figures 3 and 5). In other words, Paul relates to a processor comprising a circuitry for handling interruptions in this processor and for managing pipelines, when for example recognizing a DMA interrupt. Therefore, according to Paul, the interrupt handling is performed on the processor side.

The present invention, on the other hand, relates to data transmission from a circuitry to a processor via direct memory access by setting up at the circuitry a direct memory access for transferring data, triggering at the circuitry a direct memory access transfer of the data to the processor device, adding in the circuitry the direct memory access transfer to a transaction log, providing the transaction log from the circuitry to the processor device when the transaction log has reached a predetermined limit, and informing the processor device of the availability of the transaction log. Therefore, it is clear that, according to the present invention, the steps involved in the data transmission are performed at the circuitry side. Whereas, according to Paul the interrupt handling is performed on the processor side.

Accordingly, Applicants respectfully submit that Paul fails to disclose or suggest "setting up at said circuitry a direct memory access for transferring data; triggering at said circuitry a direct memory access transfer of said data to said processor device," as recited in claim 1, and "functionality configured to provide access to a processor device, wherein said integrated circuit is configured to set up a direct memory access for transferring data via said access means, to trigger a direct memory access transfer of said data, to add said direct memory access transfer to said transaction log," as recited in claim 11. As such, Applicants respectfully request that this rejection be withdrawn.

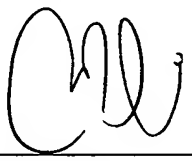
Claims 2-7, 12, and 13 are dependent upon claims 1 and 11, respectively. Consequently, claims 2-7, 12, and 13 should be allowed for at least their dependence upon claims 1 and 11, and for the specific limitations recited therein.

For at leas the reasons discussed above, Applicants respectfully submit that Paul fails to disclose or suggest all of the elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-7, 11-13 and 15 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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